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W. Lawson
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ATTORNEY'S DOCKET NO: **A1998017 (formerly A0521/7153)**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: FRINK, Craig
Serial No: 09/054,933
Filed: April 3, 1998
For: METHOD AND APPARATUS FOR ACCESSING VIDEO DATA IN MEMORY ACROSS FLOW-CONTROLLED INTERCONNECTS

Examiner: K. O. Bui
Art Unit: 2611

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Commissioner for Patents, Washington, D.C. 20231, on January 7, 2002.

Peter J. Gordon, Reg. No. 35,164

Commissioner for Patents
Washington, D.C. 20231

REPLY

Sir:

In reply to the Office Action of October 7, 2002, and in view of the following remarks, reconsideration is requested. Claims 1-10 remain in the application of which claims 1, 2, 3, 6, 9 and 10 are independent.

Rejection Under 35 U.S.C. §103

Claims 1-10 were rejected under 35 U.S.C. §103 in view of U.S. Patent 6,018,765 ("Durana") and U.S. Patent 5,819,056 ("Favor").

Independent claims 1, 2, 3, 6, 9 and 10 all recite systems having an interface (either an output or input interface) that include data, a valid data signal that indicates if the data includes valid video data, and a command valid data signal that indicates if the data includes valid command data. *One of* the valid data signal and valid command signal is asserted, depending on whether the data includes video data or command data.

Durana illustrates in Fig. 6 a decoder that has analog composite video and analog audio outputs (shown at 118 and 112/114, respectively). See col. 8, lines 16-27. The Examiner asserts that these outputs (118 and 112/114) are the claimed "output for providing video data." Durana also teaches that this decoder (labeled 14 in Fig. 2) provides outputs from decoders 20 to modulators 32, which create modulated outputs at different frequencies. See Col. 3, lines 60-65. A set top box 42 is used by a user who may, for example, select a movie by pressing a preselected button on a remote control device. See Col. 4, lines 8-10. The inputs are sent from the set top box 42 to the central control 46. The control 46 instructs the set top box 42 to tune to a specific television channel corresponding to a specific decoder video channel. The control 46 then instructs the server, which in turn commands the encoder to read the selected movie and play it on the specific decoder video channel. See Col. 4, lines 4-21.

None of the signals referred to in Col. 4, lines 4-21 (the signal from set top box 42 to control 46, or the signal 48 from control 46 to the host 10) can be understood as the claimed "valid data signal" that indicates if the data includes valid video data or as the claimed " valid command signal" that indicates if the data includes valid command data because none of the signals in Fig. 2 of Durana indicate anything about the data output from the decoders 14 in that Fig. 2. Therefore, contrary to the Examiner's assertion, the output interface of the decoder in Durana therefore cannot "assert one of the valid data signal and valid command signal to the receiver in response to a request signal received from the receiver." The decoder in Durana merely outputs the video data when instructed - there is no "valid data signal."

Favor teaches a computer processor with a set of macroinstruction decoders. Each macroinstruction decoder has "multiple reasons which are combined into decoder valid signals to determine whether that decoder is able to successfully perform a decode. The decoder valid signals for all of the decoders are then monitored, in combination, to determine the type of decode cycle to perform." See Col. 32, lines 23-28. The computer processor also includes a branch predictor that has a "branch targer buffer (BTB)." Col. 32, lines 46-47. The BTB has entries that hold instructions including a memory byte and a tag that includes an entry valid bit. Col. 33, lines 28-30. The BTB may be accessed during a decode cycle and appears to be used according to the branch prediction algorithm. See col. 33, lines 4-5. Althoug Favor teaches a processor that provides one signal, that indicates that a decoder is able to perform a decode operation, and other data in a tag of a BTB entry that indicates whether that BTB entry includes a

valid instruction, Favor does not teach an output interface that provides a) data, b) a signal indicating whether that data includes valid video data and c) a signal indicating whether that data includes valid command data and d) transferring the data over the output while asserting *one of* the valid data signal and the valid command signal.

The Examiner asserts that the system of Durana would be modified according to the teachings of Favor "to verify memory addresses at the receiver in order to provide valid data signals including valid command signal in response to a request signal at the receiver." The Applicant respectfully disagrees that one of ordinary skill in the art would modify the system of Durana (that teaches how a central multimedia server can be accessed to provide video signals to a set top box) with teachings from Favor about how a computer processor is designed to decode macroinstructions. The reason provided by the Examiner as to why such a combination would be made lacks supporting evidence from the prior art. Further it is unclear how the teachings of Favor's macroinstruction decoder and branch prediction logic could be applied to Durano's system in any way that would suggest an output interface that provides a) data, b) a signal indicating whether that data includes valid video data and c) a signal indicating whether that data includes valid command data and transferring data over that output while asserting *one of* the valid data signal and the valid command signal.

Regarding claim 9, the Examiner merely refers to the discussion of claim 1, but repeats the rejection from the prior office action, stating that Durana teaches limitations of claim 9 that the Examiner admits are not taught by Durana in the discussion of claim 1 (particularly, the "valid data signal" and "the valid command signal" and that the command data includes a memory address at the reciever). As noted in the Applicant's prior reply, in Durana a programmable logic device (PLD) 222 controls transfer of digital data to multimedia processors that produce the video outputs in Fig. 6. The Examiner asserts that "the status of data, whether it is a valid video data or not, can be determined based on their memory addresses," citing Col. 16, lines 37-66. The portion of the reference that has been cited, however, has nothing to do with indicating whether audio and video outputs of Fig. 6 are valid. The cited portion of the reference merely states that some inputs to the PLD indicate that an address on an address bus is valid. See Col. 16, lines 62-64. Such an *input* to the PLD is not a signal that is part of an interface that includes the video output of Fig. 6. The Examiner also asserts that "the command data is a memory address at the receiver," citing Col. 5, lines 55-67. This data has nothing to do with the

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For:	Method And Apparatus for Accessing Video Data In Memory Across Flow-Controlled Interconnects		
Inventor:	Craig R. Frink		

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Peter J. Gordon, Reg. No. 35,164

Assistant Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL LETTER

Transmitted herewith for filing in the above-entitled patent application is a Reply to the Office Action mailed October 7, 2002.

No fees are required. The Commissioner is hereby authorized to charge **Deposit Account No. 50-0876** for any fees which may be required or credit any overpayment. A duplicate copy of the sheet is enclosed.

Dated: January 7, 2003

Respectfully submitted,

Peter J. Gordon
Registration No. 35,164
Attorney for Applicant
Avid Technology, Inc.
One Park West
Tewksbury, Massachusetts 01876
Tel. 978-640-3011